LF – 50 MHz Dual I/Q Demodulator and Phase Shifter

PRELIMINARY TECHNICAL DATA

AD8333

FEATURES

Dual Integrated I/Q Demodulator
16 Phase Select on each Output (22.5° per step)
Quadrature Demodulation Accuracy
- **Phase Accuracy ±0.5°**
- **Amplitude Balance ±0.1 dB**

Bandwidth
- **4LO: LF – 200 MHz; RF: LF - 50 MHz**
- **Baseband: determined by external filtering**

Output Dynamic Range 161 dB/Hz
LO Drive > 0 dBm (50 Ω); 4 LO>1MHz
Supply: ±5 V
Power Consumption 190 mW/channel (380 mW total)
Power Down

APPLICATIONS

Medical Imaging (CW Ultrasound Beamforming)
Phased Array Systems
- **Radar**
- **Adaptive Antennas**

Communication Receivers

GENERAL DESCRIPTION

The AD8333 is a dual base-band phase shifter and I/Q demodulator. It is the worlds first solid state device suitable for beamformer circuits, such as used in high-performance medical ultrasound equipment featuring CW Doppler. The RF inputs have been designed to interface directly with the differential outputs of dual-channel low-noise pre-amplifiers as in the AD8332 VGA. A divide-by-four circuit divides the 4X local oscillator (LO) input signal and generates the 0° and 90° phases of the LO that drive the mixers of a pair of well-matched I/Q demodulators.

A major application is in medical ultrasound imaging, particularly continuous wave (CW) analog beamforming. The AD8333 enables coherent summing and phase alignment of multiple input channels. A reset pin synchronizes an array of AD8333s so that they start in the same quadrant. Sixteen discrete phase rotations in 22.5° increments can be selected independently for each channel. For example, if CH1 is used as a reference and CH2 has an I/Q phase lead of 45°, then by choosing the correct code one can phase align CH2 with CH1.

The I and Q mixer outputs are provided as currents to facilitate summation. The summed current outputs are converted to voltages by a high dynamic-range current-to-voltage (I-V) converter, such as an AD8021, configured as a transimpedance amplifier. The resultant signal is then applied to a high resolution AD converter (ADC) such as the AD7665 (16b/570 ksps).

FUNCTIONAL BLOCK DIAGRAM

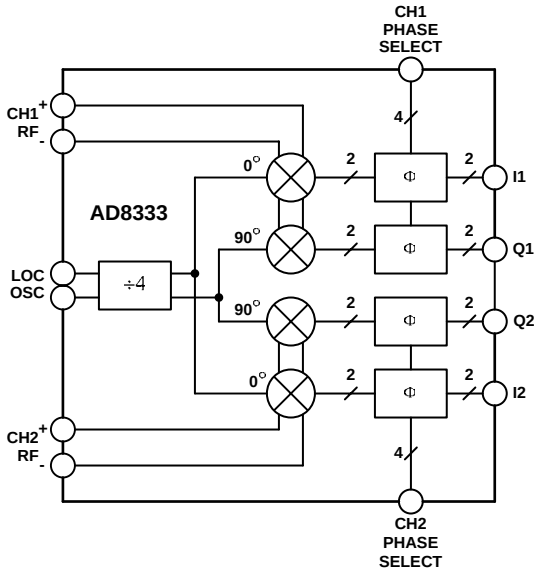

Figure 1.

The two I/Q demodulators can also be used independently in other non-beamforming applications. In that case a transimpedance amplifier is needed for each of the I and Q outputs - four in total for the dual I/Q demodulator.

The dynamic range is 161 dB/Hz at the I and Q outputs, but the following transimpedance amplifier is an important element in maintaining the overall dynamic range and attention needs to be paid to optimal component selection and design.

The AD8333 is available in a 32 pin LFCSP (5x5 mm) package for the industrial temperature range of -40 C to +85 C.

REV. PrB 4/29/2005

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REVISION HISTORY

Rev. PrA:

AD8333—ADVANCE SPECIFICATIONS

Table 1. V_S = ±5 V, T_A = 25°C, $4f_{LO}$ = 20 MHz, f_{RF} = 5.01 MHz, f_{BB} = 10 kHz, P_{LO} ≥ -10 dBm, per channel performance, dBm (50 Ω) unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	4x internal LO at pins 4LOP and 4LON	LF		200	MHz
RF Frequency Range	Mixing	LF		50	MHz
Baseband Bandwidth	Limited by external filtering	LF		50	MHz
LO Input Level		-10		13	dBm
V_{SUPPLY} (V_S)		TBD	±5	TBD	V
Temperature Range		-40		+85	°C
DEMODULATOR PERFORMANCE					
Input Impedance	RF - Differential		11||TBD		kΩ||pF
	LO – Differential		TBD||TBD		kΩ||pF
Transconductance	Demodulated I_{OUT}/V_{IN}, each Ix or Qx output after low pass filtering measured from RF inputs				
	All phases		2.17		mS
Dynamic Range	IP1dB – Input Referred Noise (dBm)		161		dB/Hz
Max RF Input Swing	Differential; Inputs biased at 2.5V; Pins RFxP, RFxN		2.8		Vpp
Peak Output Current (no filtering)	PHx0=PHx1=0 --> 0° Phase Shift		±4.7		mA
	PHx0=PHx1=1 --> 45° Phase Shift		±6.6		mA
Input P1dB	Ref = 50 Ω		14.5		dBm
	Ref = $1V_{RMS}$		1.5		dBV
Third Order Intermodulation (IM3)	f_{RF1} = 5.010 MHz, f_{RF2} = 5.015 MHz, f_{LO} = 5.023MHz				
Equal Input Levels	Baseband Tones = -7dBm @ 8kHz and 13 kHz		-75		dBc
Unequal Input Levels	Baseband Tones: -1dBm @ 8kHz and -31dBm @ 13 kHz		TBD		dBc
Third Order Output Intercept (OIP3)	Same conditions as equal level IM3		30		dBm
LO Leakage	Measured at RF Inputs, worst phase, measured into 50Ω		<-100		dBm
	Measured at Baseband Outputs, worst phase, 8021 disabled, measured into 50Ω		-60		dBm
Conversion Gain	Measured with Test Circuit 1; all codes		4.7		dB
Input Referred Noise	Output Noise from Test Circuit 1/Conversion Gain		11		nV/√Hz
Noise Figure	With AD8332 LNA, R_S = 50 Ω, R_{FB} = ∞		TBD		dB
	R_S = 50 Ω, R_{FB} = 275 Ω		TBD		dB
	R_S = 50 Ω, R_{FB} = 1.1k Ω		TBD		dB
	AD8333 only; R_S = 50 Ω, no termination on RFxP, RFxN		TBD		dB
Bias Current	Pins 4LOP, 4LON		TBD		µA
	Pins RFxP, RFxN		TBD		µA
LO Voltage Range	Pins 4LOP, 4LON (each pin)	TBD		TBD	V
RF Common Mode Voltage	For maximum differential swing; Pins RFxP, RFxN		2.5		V
Output Compliance Range	Pins IxPO, QxPO	TBD		TBD	V
PHASE ROTATION PERFORMANCE	One CH is reference, other is stepped				
Phase Increment	16 Phase Steps per Channel		22.5		°
Quadrature Phase Error	I1 to I2 and I2 to Q2		±0.5		°
I/Q Amplitude Imbalance	I1 to I2 and I2 to Q2		±0.1		dB
Channel-to-Channel Matching	Phase Match I1/I2 and Q1/Q2		±1		°
	Phase Match I1/I2 and Q1/Q2; -40°C < T_A < 85°C	±TBD		±TBD	°

Parameter	Conditions	Min	Typ	Max	Unit
	Amplitude Match I1/I2 and Q1/Q2		±0.5		dB
	Amplitude Match I1/I2 and Q1/Q2; -40°C < T_A < 85°C	TBD		TBD	dB
LOGIC INTERFACES	Pins PHxx, RSET and ENBL				
Logic Level High		TBD		TBD	V
Logic Level Low		TBD		TBD	V
Bias Current	Logic High		TBD		µA
	Logic Low		TBD		µA
Input Resistance	Pins PHxx and ENBL		TBD		kΩ
	Pin RSET		TBD		kΩ
Reset Setup Time	Reset is asynchronous		TBD		ns
Reset Response Time			TBD		µs
Phase Response Time			TBD		µs
Enable Response Time			TBD		µs
POWER SUPPLY	Pins VPOS,VNEG				•
Supply Voltage			±5		V
Quiescent Current	VPOS, PHx0=PHx1=0	TBD	44	TBD	mA
	VNEG, PHx0=PHx1=0	TBD	21	TBD	mA
Over Temperature	-40°C < T_A < 85°C	TBD		TBD	mA
Quiescent Power	Per Channel (PHx0=PHx1=0)		170		mW
	Per Channel (PHx0=0, PHx1=1)		190		mW
Disable Current	All Channels Disabled		TBD		µA
PSRR	VPOS to Ix/Qx outputs (meas. @ AD8021 output)		TBD		dB
	VNEG to Ix/Qx outputs (meas. @ AD8021 output)		TBD		dB

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8333 Absolute Maximum Ratings

Parameter	Rating
Voltage s	
Supply Voltage V_S	6V
RF Pin Inputs	TBD V
LO Inputs	TBD V
Code select InputsV	TBDV
Thermal Data (No Airflow)	
θ_{JA}	41.0°C/W
θ_{JB}	23.6°C/W
θ_{JC}	4.4°C/W
Ψ_{JT}	0.4°C/W
Ψ_{JB}	22.4°C/W
Maximum Junction Temperature	TBD°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

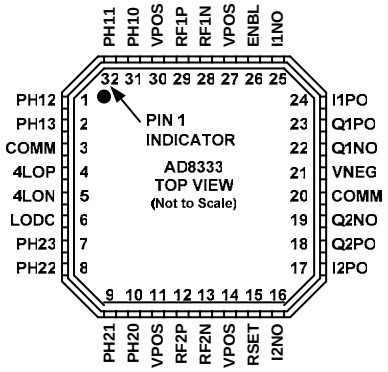

Figure 2. 32-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function	Equiv. Circ.
1, 2, 7, 8	PH12, PH13 PH22, PH23	Quadrant Select LSB,MSB. Binary Code. These logic inputs select the quadrant: 0-90, 90-180, 180-270, 270-360°. See table in Theory of Operation section. Logic threshold is at about 1.5V and therefore can be driven by 3V CMOS logic.	A
3, 20	COMM	Ground. These two pins are internally tied together.	
4, 5	4LOP, 4LON	LO Inputs. No internal bias, therefore these pins need to be biased by external circuitry. For optimum performance these inputs should be driven differentially with a signal level that is not less than shown in figure 25B, minimum LO level vs RF. Bias current is only –3 μA. Single ended drive is also possible if the inputs are biased correctly.	B
6	LODC	Decoupling pin for LO. A 0.1μF capacitor should be connected between this pin and ground.	C
9, 10, 31, 32	PH20, PH21 PH10, PH11	Phase Select LSB,MSB. Binary Code. These logic inputs select the phase for a given quadrant: 0, 22.5, 45, 67.5°. See table in Theory of Operation section. Logic threshold is at about 1.5V and therefore can be driven by 3V CMOS logic.	A
11, 14, 27, 30	VPOS	Positive Supply. These pins should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μF and 100 pF capacitor between the VPOS pins and ground. Since the VPOS pins are internally connected, one set of supply decoupling components for all four pins should be sufficient.	
12, 13, 28, 29	RF2P, RF2N RF1P, RF1N	RF Inputs. These pins are biased internally, however it is recommended that they are biased by dc coupling to the output pins of the AD8332 LNA. The optimum common mode voltage for maximum symmetrical input differential swing is 2.5V if ±5V.supplies are used.	D
15	RSET	Reset for divide-by-four in LO interface. Logic threshold is at about 1.5V and therefore can be driven by 3V CMOS logic.	A
16, 19, 22, 25	I2NO, Q2NO I1NO, Q1NO	Negative I/Q outputs. These outputs are not connected for normal usage, but can be used for filtering if needed. Together with the positive I/Q outputs, they allow bypassing the internal current mirror if a lower noise output circuit is available; VNEG needs to be tied to GND to disable the current mirror.	E
17, 18, 23, 24	I2PO, Q2PO I1PO, Q1PO	Positive I/Q Outputs. These are the outputs which provide a bidirectional current that can be converted back to a voltage via a trans-impedance amplifier. Multiple outputs can be summed together by simply connecting them together. The bias voltage should be set to 0V or less by the transimpedance amplifier.	E
21	VNEG	Negative Supply. This pin should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μF and 100 pF capacitor between the pin and ground.	
26	ENBL	Chip Enable. Logic threshold is at about 1.5V and therefore can be driven by 3V CMOS logic.	A

Device Input Equivalent Circuits

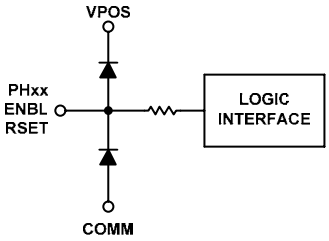

Figure 3. Logic Inputs

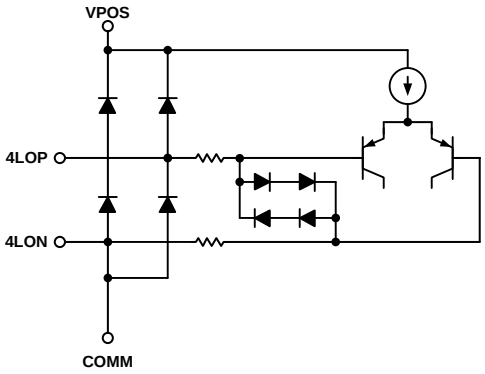

Figure 4. Local Oscillator Inputs

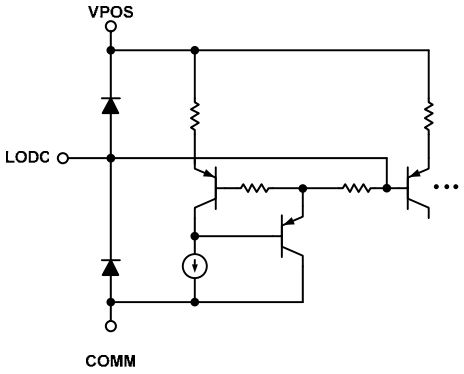

Figure 5. Circuit C

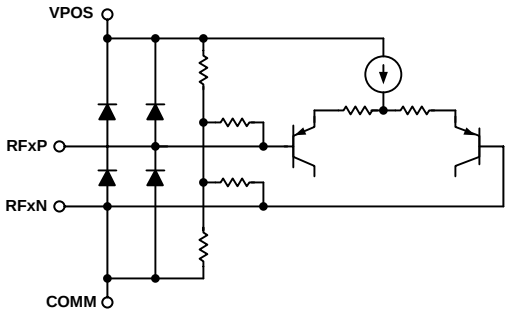

Figure 6. RF Inputs

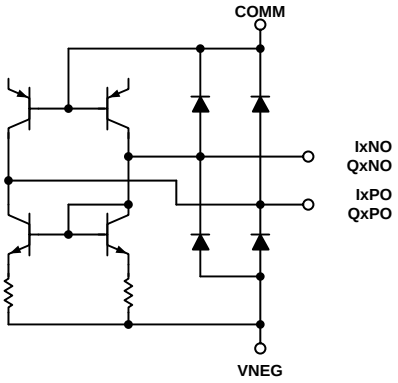

Figure 7. Output Drivers

THEORY OF OPERATION

OVERVIEW

The AD8333 is a dual I/Q demodulator with programmable phase shifter for each channel. The primary applications are: phased array beamforming in medical ultrasound; phased array radar; smart antennas for mobile communications. The part could also be used in applications that require two well matched I/Q demodulators.

Figure 8 shows the basic block diagram and the pinout of the AD8333. The device requires only 3 inputs: a Local Oscillator (LO) signal common to both channels and RF sources for channels 1 and 2. Each channel features independent phase delay circuitry; there are 16 states/360 degrees (or 22.5°/step). selectable with the PHx0-PHx3 logic inputs.

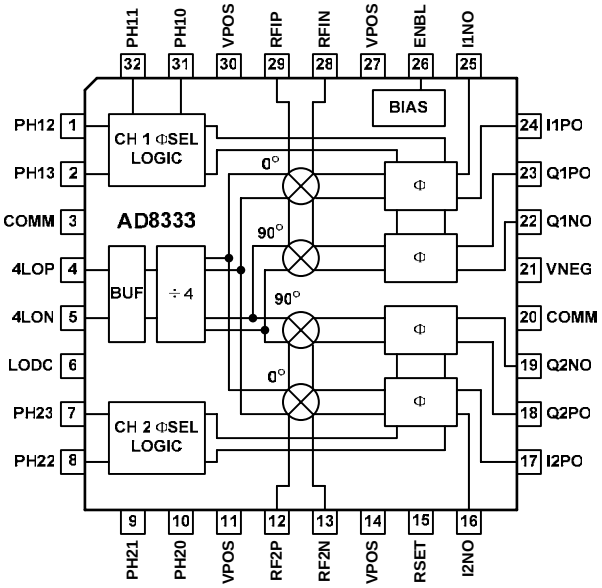

Figure 8 Block diagram and pinout

The outputs are in current form to allow for easy summation in beamforming applications. Multiple channels can be summed and then need to be converted to a voltage using a transimpedance amplifier. Of course, the channels can also be used individually.

QUADRATURE GENERATION

The internal 0° and 90° LO phases are digitally generated by a divide-by-4 logic circuit. The divider is dc coupled and inherently broadband, its maximum LO frequency limited only by its switching speed. The duty cycle of the quadrature LO signals is always 50% and is not affected by asymmetry of the externally connected 4xLO input. Furthermore, the divider is implemented such that the 4xLO signal re-clocks the final flip-flops that generate the internal LO signals and thereby minimizes noise introduced by the divide circuitry. For optimum performance, the LO input is driven differentially, but can be driven single-ended if desired; a good choice for drive is LVDS. The common-mode range on each pin is approximately 0.5 to 3.3 V with nominal ±5 V supplies.

The minimum LO level is frequency dependent (refer to Figure 25B). For the best noise performance it is of great importance to insure that the LO source has very low phase noise (jitter) and adequate input level to assure stable mixer-core switching.

Because in a beamforming application many channels are coherently summed and the coherence depends on an accurate phase relationship between channels, a reset pin (RSET) is provided to help synchronize the divide-by-4s in different AD8333s. The RSET pin resets the counters to a known state, without it, when multiple AD8333s are powered up, the LO dividers might come up in different quadrants which can cause a 90, 180, or 270° degree phase error relative to another part. It is therefore important to reset the dividers when using more than one AD8333.

I/Q DEMODULATORS AND PHASE SHIFTERS

The I/Q demodulators consist of double-balanced Gilbert cell mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability of 2.8 Vpp. These currents are then presented to the mixers which convert them to baseband: RF-LO and RF+LO. Following down-conversion the signals are phase shifted according to the code applied to the PHx0-PHx3 pins (see Table 4). After the phase shifters, the differential current signal is converted from differential to single-ended via a current mirror. The single-ended outputs (I1PO, I2PO, Q1PO, Q2PO) can then be converted back to a voltage via a transimpedance amplifier as done on the evaluation board.

PHx3	PHx2	PHx1	PHx0	ϕ-Shift
0	0	0	0	0°
0	0	0	1	22.5°
0	0	1	0	45°
0	0	1	1	67.5°
0	1	0	0	90°
0	1	0	1	112.5°
0	1	1	0	135°
0	1	1	1	157.5°
1	0	0	0	180°
1	0	0	1	202.5°
1	0	1	0	225°
1	0	1	1	247.5°
1	1	0	0	270°
1	1	0	1	292.5°
1	1	1	0	315°
1	1	1	1	337.5°

Table 4 .Phase Shift of Channel-to-Channel with one Channel as Reference

LOGIC INTERFACES

The logic interfaces, PHxx, ENBL and RSET all have a threshold of VPOS*0.3. This means that in the case of a 5V supply, the threshold will be at about 1.5V; there is some built in hysteresis

around this value.

DYNAMIC RANGE AND NOISE

Figure 9 is a block diagram showing external connections to the AD8333. Typically the RF inputs are driven from a very low noise amplifier like the LNA in the AD8332 family or the preamplifier in the AD8335. Note also that in this diagram the outputs for the two channels are shown connected (summed), this improves the dynamic range by 3 dB assuming that the noise sources of the two channels are uncorrelated. In general the dynamic range improvement is 10*log10(N) where N is the number of channels that are summed together.

To ensure that the dynamic range is reduced as little as possible, it is important that the amplifier that drives the AD8333 is carefully selected. The input referred noise per channel of the AD8333 is about 9 nV/√Hz; if the noise of the AD8333 should only degrade the overall noise figure (NF) by about 1 dB then the noise of the source and the LNA should be about twice that value at 18 nV/√Hz. If the noise of the circuitry before the AD8333 is lower than that then the NF degrades more than 1 dB, for example, if the noise is equal at 9 nV/√Hz then there will be a 3 dB degradation; if it is 1.3 times as big (about 11.7 nV/√Hz) then there will be a 2 dB degradation; at 1.45 times as large (13.1 nV/√Hz) it would be a 1.5 dB degradation.

To determine the input referred noise it is important to know the active LPF (low pass filter) values, shown in Figure 47 as R_{FILT} and C_{FILT}. On the AD8333 evaluation board they are 787Ω and 2.2 nF respectively, implementing a 90 kHz single pole LPF. If the RF and LO are offset by 10 kHz, then the demodulated signal will be 10 kHz; the mixing gain after low pass filtering, from one of the RF inputs to the AD8021 output when measuring a single output only (i.e. I1, Q1, etc.) is approximately 1.7x (4.7dB). This together with the 9 nV/√Hz AD8333 noise results in about 15.3 nV/√Hz at the AD8021 output. Since the AD8021, including the 787 Ω feedback resistor, contributes another 4.4 nV/√Hz, the total output referred noise will be about 16 nV/√Hz. This value can be adjusted by increasing the filter resistor, thereby increasing the gain

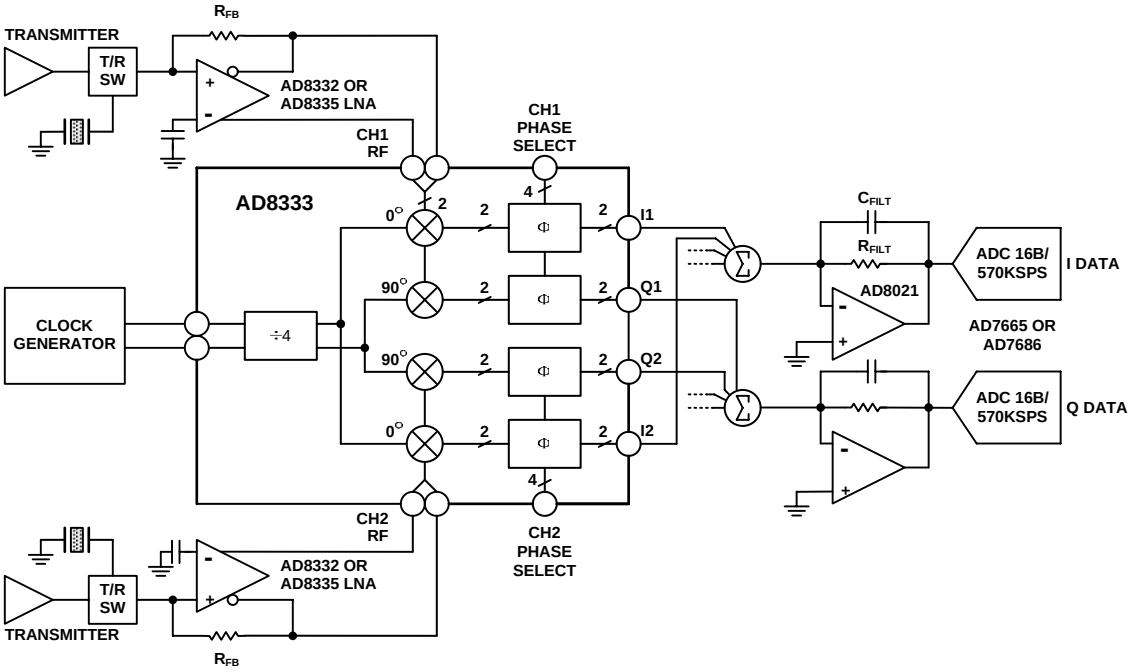

Figure 9. Connection Block Diagram

BYPASSING CURRENT MIRROR AND DECREASING NOISE

The noise contribution of the AD8333 can be reduced if the current mirrors that convert the internal differential signals to single-ended are bypassed (see Figure 10). Current mirrors interface to the AD8021 current-to-voltage (I-V) converters shown in Figure 9, and provide low-pass filtering. The AD8021s force the AD8333 output voltage to 0V, and process the bipolar output current, however the mirrors introduce a significant amount of noise. This noise may be reduced if they are bypassed and externally biased.

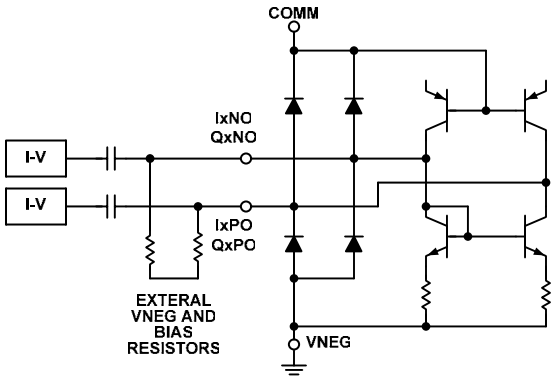

Figure 10 Bypassing the Internal Current Mirrors

The mirrors are disabled by connecting VNEG to ground, and providing external bias networks as shown in Figure 10. The larger the drop across the resistors, the less noise they will contribute to the output, however the voltage on the IxxO and QxxO nodes cannot exceed +0.5 V. Voltages exceeding approximately 0.7 V will turn on the PNP devices, and forward bias the ESD protection diodes. Inductors provide an alternative to resistors, enabling reduced static power by eliminating the power dissipation in the bias resistors. With inductors the main limitation might be low frequency operation, as is the case in CW Doppler in ultrasound where the frequency range of interest goes from a few hundred Hertz to about 30 kHz. In addition it is still important to provide enough gain through the I-V circuitry to ensure that the bias resistor and I-V converter noise does not contribute significantly to the noise from the AD8333 outputs.

As should be obvious from Figure 10, the main disadvantage of the external bias approach is that now two I-V amplifiers are needed because of the differential output. For beamforming applications the outputs would still be summed as before but now there are twice the number of lines. Only two bias resistors are needed for all outputs that are connected together. The resistors would be scaled by dividing the value of a single output bias resistor through N – the number of channels connected in parallel. The bias current depends on the phase selected: for phase 0° this is about 2.5 mA per side, while in the case of 45° this is about 3.5 mA per side. The bias resistors should therefore be chosen based on the larger bias current value of 3.5 mA and the chosen VNEG. VNEG should be at least -5 V, and may be larger for additional noise reduction.

APPLICATIONS

The AD8333 is the key component of a phase-shifter system used to align time-skewed information contained in RF signals. It is important to consider the many I/O options necessary to perform it's intended function.

Figure 11 shows the basic connections. For maximum input swing, the RF inputs (pins 12,13,28 and 29) are dc coupled to the differential output of the LNA section of the AD8331/2 series of Variable Gain Amplifiers.

Figure 12 and Figure 13 show the Evaluation Board schematic; it includes the AD8332 to allow tests either directly as one would use it in an actual application or by applying signals via connectors directly to the RF inputs. For best performance it is recommended that the RF inputs are driven differentially. Although the 4XLO input can be driven single-ended, differential is recommended. The 4XLO inputs require very low bias currents and can be supplied by a multi-drop LVDS driver, or LV-PECL, or any other high speed differential signal that stays within the common-mode range of the inputs (0.5 to 3.3 V).

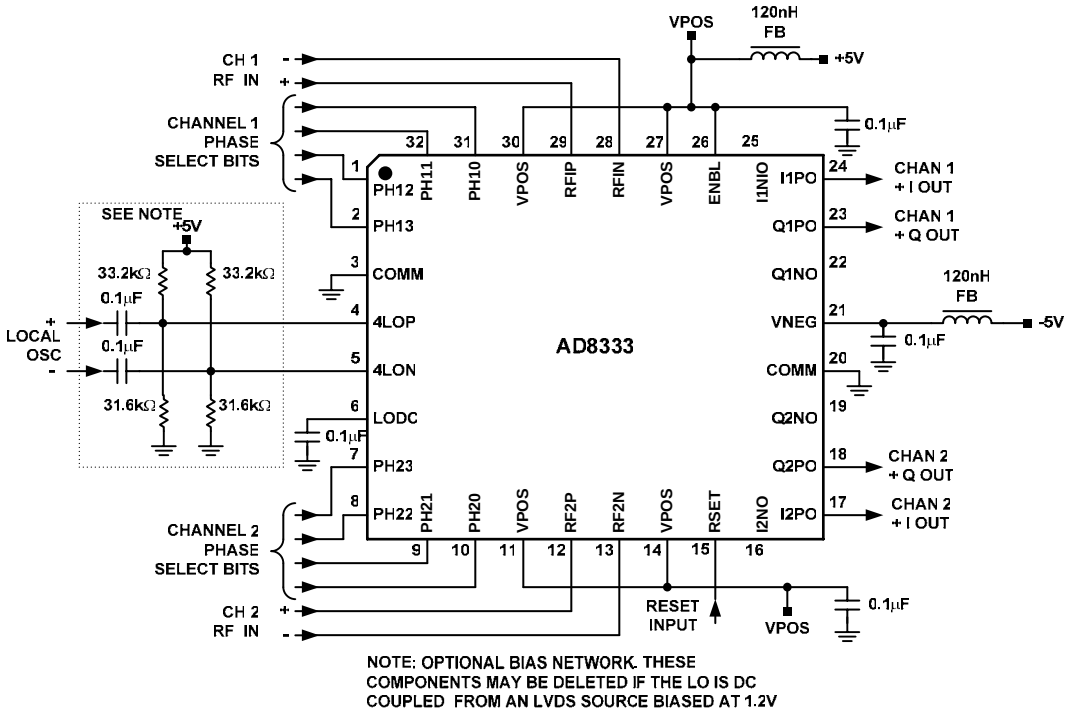

Figure 11. AD8333 Basic Connections

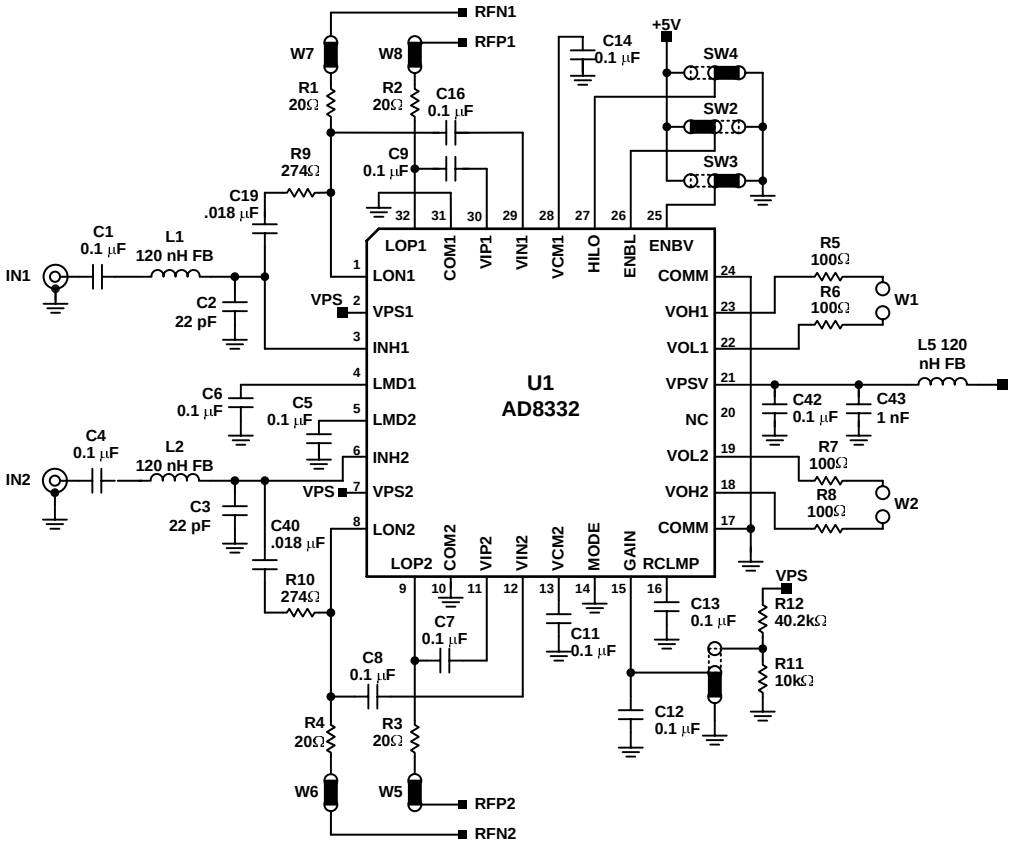

Figure 12. AD8333 Eval Board Schematic- LNA

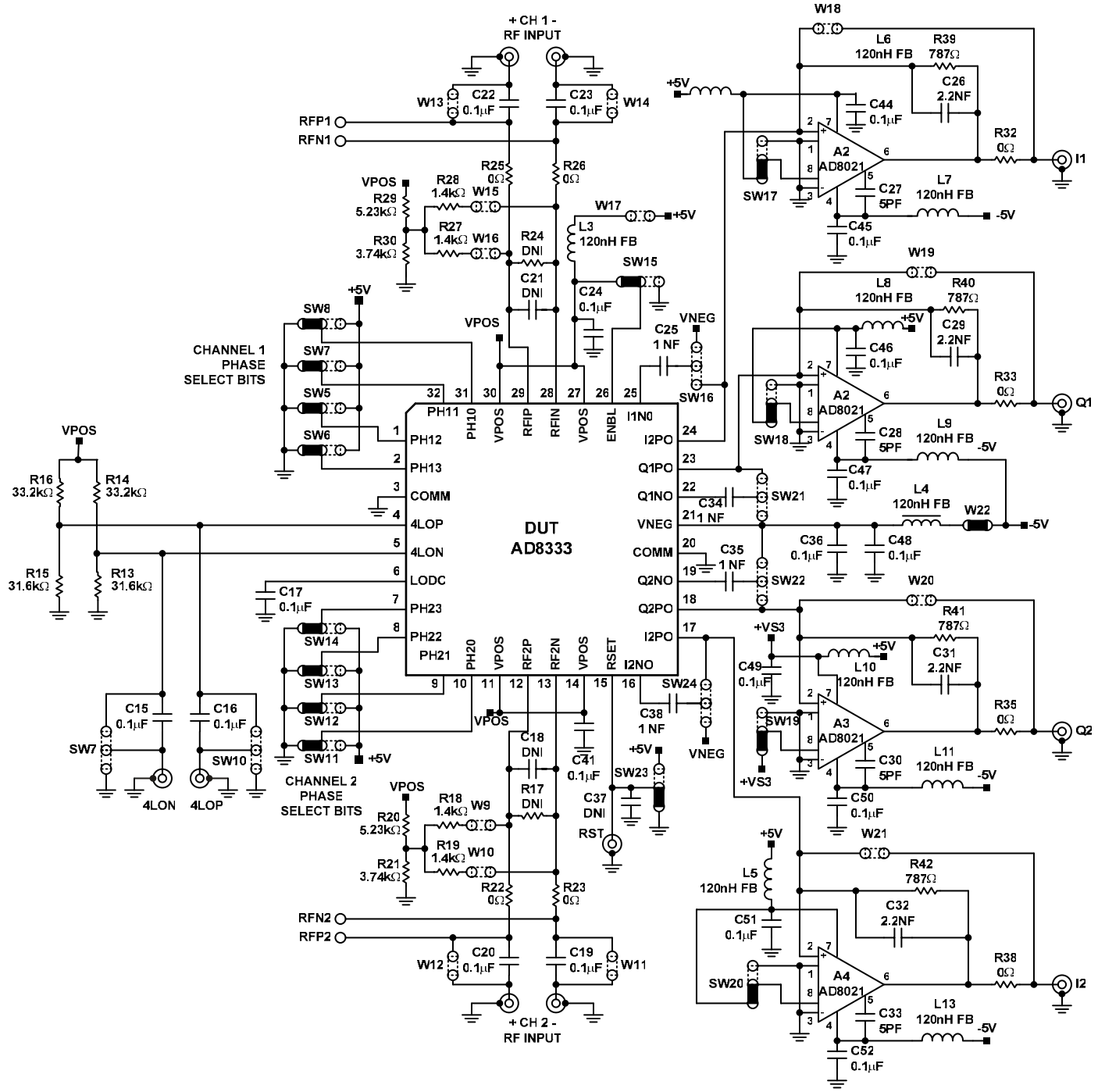

Figure 13. Eval Board Schematic - AD8333

OUTLINE DIMENSIONS

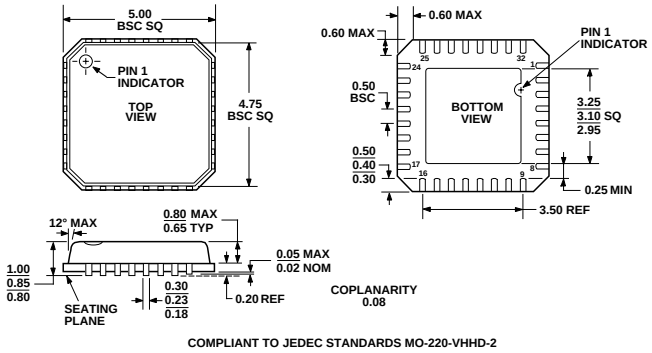

Figure. 32-32-Lead Frame Chip Scale Package [LFCSP] (CP-32)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8333ACPZ-REEL	–40°C to +85°C	32-Lead Chip Scale	
AD8333ACPZ-REEL7	–40°C to +85°C	32-Lead Chip Scale	
AD8333-WP	–40°C to +85°C	32-Lead Chip Scale	
AD8333-EVAL			

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